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TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			EXAMINER WELLS, KENNETH B	
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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 10/614,846

Filing Date: July 08, 2003

Appellant(s): TORRES, HECTOR

W. Daniel Swayze, Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/2/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

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(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct. This appeal involves claims 1-15.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

The amendment after final rejection filed on 1/21/05 has been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

U.S. Patent No. 4,992,681 (Urakawa et al) Feb. 1991

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 13-15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Urakawa et al.

As to claim 1, note Fig. 6, where the recited "differential first pair of transistors" reads on BJTs Q2 and Q3; the recited "voltage drive stage" reads on BJTs Q8 and Q9; the recited "first pair of nodes" reads on the collectors of Q2, Q3; the recited "second pair of nodes" reads on the emitters of Q8, Q9; and the recited "dynamic current switch" reads on the combination of Q10, Q11 and current source I5.

As to claim 2, the recited resistors read on R1 and R2 of Urakawa et al's Fig. 6 circuitry.

As to claims 13 and 14, the recited operation is seen to be inherent in Urakawa et al's Fig. 6 circuitry.

As to claim 15, the recited pair of input nodes read on the nodes which receive signals B and V1.

Claims 3-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakawa et al.

As to claim 3, the use of voltage regulators in integrated circuits is old and well-known in the art for obtaining well-known benefits (of which fact official notice is taken by the examiner). Thus, claim 3 does not distinguish patentably over Urakawa et al.

The same is true for claims 4 and 5, since load resistors are also notoriously old and well-known in the art (put into the legs of differential stages for the well-known purpose of current limiting).

As to claims 6 and 7, the output voltage is the differential signal D, /D and the output nodes are the nodes which receive these voltage signals.

Claims 8 and 11 also fail to define patentable subject matter over Urakawa et al because making the three current

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sources I1, I2 and I5 using a serial connection of a resistor and transistor would have been obvious to any person having ordinary skill in the art because (1) the claimed structure is old and well-known and (2) there is motivation to use such a structure for each of the generic current sources taught by Urakawa et al (i.e., to obtain the well-known advantages of such well-known structures). The input node of claim 8 reads on the node receiving signal A in Urakawa et al's Fig. 6 circuitry.

As to claims 9 and 10, note that all points in the circuit of Urakawa et al are electrically connected to each other either directly or through intervening circuit elements.

In claim 12, the recited transistor reads on BJT Q1 in Urakawa et al's Fig. 6 circuitry.

(10) Response to Argument

Appellant's first argument is at page 3, lines 18-19 of the brief is that "no differential signal or consequently the differential first pair of transistors is seen." This argument is without merit because a differential signal is not required to anticipate the claims (i.e., the recited input signal is not part of the invention, it is merely intended use and thus cannot be relied upon to distinguish over Urakawa et al). The further assertion by appellant, that "no... differential first pair of

transistors is seen" is also without merit, i.e., BJTs Q2 and Q3 in Urakawa et al are clearly differentially coupled transistors.

Appellant's next argument, at the top of page 4 of the brief, is that "the differential signal is part of the claimed invention..." As noted above, this statement is without merit because the claims are directed to a circuit, and the signal applied to the circuit is clearly not part of the circuit. Thus the recitation of the type of input signal is merely intended use and cannot be relied upon to define over Urakawa et al because the reference is of course capable of receiving such an input signal.

Finally, it is not speculation, as asserted by appellant, to conclude that the Urakawa et al Fig. 6 circuit is capable of receiving a differential input signal (because it is common knowledge in the art that differentially coupled transistors, such as BJTs Q2 and Q3 of Urakawa et al, can indeed receive complementary (differential) input signals.

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(11) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kenneth B. Wells
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August 2, 2005

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